REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 2-8 and 18, 27, and 36-39 are in this application. Claims 18, 27, and 36 have been amended. Claims 11-17, 19-26, 28-35, and 40-44 have been cancelled.

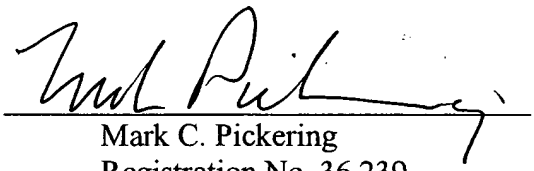
The Examiner rejected claims 11, 20, and 29 under 35 U.S.C. §251 as being an improper recapture of subject matter that was surrendered in the application for the patent upon which the present reissue is based. In addition, the Examiner rejected claims 11-17, 19-26, 28-35, and 40-44 under 35 U.S.C. §103(a) as being unpatentable over Parruck et al. (U.S. Patent No. 4,799,144) in view of Akagi et al. (U.S. Patent No. 4,467,414). As noted above, claims 11-17, 19-26, 28-35, and 40-44 have been cancelled.

The Examiner noted that claims 2-8 and 37-39 are allowable over the prior art of record. The Examiner also objected to claims 18, 27, and 36 as being dependent upon a rejected base claim, but noted that the claims would be allowable if amended to include the limitations of the base claim and any intervening claims. Claims 18, 27, and 36 have been amended to be in independent form, and include the limitations of the base claims.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

PILLSBURY WINTHROP LLP

Dated: 10-19-01 By: 

Mark C. Pickering
Registration No. 36,239

Attorney for Assignee

50 Fremont Street, Fifth Floor
San Francisco, CA 94105-2228
Direct Dial Telephone No. (415) 983-1297
Telephone: (415) 983-1000
Facsimile: (415) 983-1200

APPENDIX

In the Claims

Please cancel claims 11-17, 19-26, 28-35, and 40-44.

Please amend the claims as follows:

18. (Amended) [The data processing system of claim 11 wherein] A data processing system comprising:

a first bus;

a memory connected to the first bus;

a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and

a digital signal processor (DSP) connected to the first bus, the DSP having a register and starting execution of an instruction in response to the GPP loading information into the register, the DSP only [executes] executing a single instruction when said information is loaded into the register.

27. (Amended) [The data processing system of claim 20 wherein] A data processing system comprising:

a first bus;

a memory connected to the first bus;

a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and

a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction, the DSP only [executes] executing a single instruction when said information is loaded into the register.

36. (Amended) [The data processing system of claim 29 wherein] A data processing system comprising:

a first bus;

a memory connected to the first bus;

a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and

a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register, the DSP only [executes] executing a single instruction when said information is loaded into the register.